IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Dimitry Gorinevsky **EXAMINER:** Nathan J. Bloom

SERIAL NO.: 10/749,694 **GROUP:** 2624

FILED: December 29, 2003 **ATTY DKT NO.:** H0006745

TITLE: IMAGE DEBLURRING WITH A SYSTOLIC ARRAY PROCESSOR

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REPLY TO FINAL OFFICE ACTION
AND
REQUEST FOR RECONSIDERATION
UNDER 37 C.F.R. § 1.111

Dear Sir:

In response to the Final Office Action dated August 18, 2008 in the above captioned matter, please enter the following remarks:

Claims begin on Page 2 of this Paper.

Remarks begin on Page 8 of this Paper.

This reply is being filed within the two-month shortened statutory period for reply.

CLAIMS

The claims are listed as follows:

1. (Previously Amended) A method of deblurring a video image, comprising the steps of:

downloading a blurred video image comprising a plurality of pixels into a systolic array processor, said systolic array processor comprising an array of processing logic blocks in parallel such that groups of said plurality of pixels arrive in each processing logic block of said array of processing logic blocks respectively;

sequentially exchanging data between said array of processing logic blocks by interconnecting said each processing logic block with only a predefined number of processing logic blocks adjacent thereto;

providing an iterative update of said blurred video image by storing each pixel of said plurality of pixels in three planes within said systolic array processor wherein said iterative update occurs within said blurred video image video frame update rate; and

uploading a deblurred video image.

2. (Previously Amended) The method of claim 1, wherein said three planes comprises said blurred video image, a blurred video image prediction error and a past deblurred video image wherein said array of processing logic blocks provide said iterative update of said blurred video image by (i) providing feedback of said blurred image prediction error using said deblurred video image and (ii) providing feedback of said past deblurred image estimate.

3. (Previously Amended) The method of claim 2, wherein said iterative update is implemented in said each processing logic block by $u(n + 1) = u(n) - K*(H*u(n)$

-- y_b) -- $S * u(n)$ where u comprises an ideal undistorted image, m and n comprise column and row indices of an image pixel element, $y_b\ (m,n)$ comprises an observed blurred image, * denotes a 2-D convolution, K comprises a feedback update operator with a convolution kernel $k(m,n)$ and S comprises ~~is~~ a smoothing operator with a convolution kernel $s(m,n)$.

4. (Previously Amended) The method of claim 2, wherein said iterative update is implemented in said each processing logic block by $u(n + 1; c) = u(n; c) -- K *(H *u(n; c) --y_b (c)) -- S * u(n;c)$ where $y_b\ (c) = y_d\ (j,k;c)$ comprises a 2-D array of color c intensities for said blurred video image encompassing all pixels (j,k) in said blurred video image and $u(n; c) = u(j,k,n;c)$ comprises a 2-D array of color c intensities for a restored image estimate at iteration number n.

5. (Previously Amended) The method of claim 1, wherein each group of said groups of said plurality of pixels comprises at least one pixel.

6. (Previously Amended) The method of claim 5, wherein said groups of said plurality of pixels comprises a group selected from 2 by 2 pixels, 3 by 3 pixels, and 4 by 4 pixels.

7. (Previously Amended) A device for deblurring an image, comprising:

a blurred video image source comprising a plurality of pixels;

a systolic array processor adapted to download said blurred video image, said systolic array processor comprising an array of processing logic blocks in parallel such that groups of said plurality of pixels arrive in each processing logic block of said array of processing logic blocks respectively, wherein said processor is adapted to sequentially exchange data between said array of processing logic blocks by interconnecting each processing logic block of said plurality of processing

logic blocks with only a predefined number of processing logic blocks adjacent thereto and wherein said systolic array processor is adapted to provide an iterative update of said blurred video image by storing each pixel of said plurality of pixels in three planes within said systolic array processor wherein said iterative update occurs within said blurred video image video frame update rate, and wherein said systolic array processor is further adapted to upload a deblurred video image.

8. (Previously Amended) The device of claim 7, wherein said three planes comprises said blurred video image, a blurred video image prediction error and a past deblurred video image and wherein said processor is adapted to provide an iterative update of said blurred video image by (i) providing feedback of said blurred video image prediction error using said deblurred video image and (ii) providing feedback of said past deblurred video image estimate.

9. (Previously Amended) The device of claim 8, wherein said systolic array processor includes an iterative update implemented in said each processing logic block by $u(n + 1) = u(n) - K *(H *u(n) - y_b)S* u(n)$ where u comprises an ideal undistorted image, m and n comprise column and row indices of an image pixel element, $y_b (m,n)$ comprises an observed blurred image, * denotes a 2-D convolution, K comprises a feedback update operator with a convolution kernel $k(m,n)$ and S comprises a smoothing operator with a convolution kernel $s(m,n)$.

10. (Previously Amended) The device of claim 9, wherein said operators H, K, and S are preloaded in said each processing logic block.

11. (Previously Amended) The device of claim 8, wherein said iterative update is implemented in said each processing logic block by $u(n + 1; c) = u(n; c) - K *(H *u(n; c) - y_b (c)) - S * u(n;c)$ where $y_b (c) = y_d (j,k;c)$ comprises a 2-D array of color c intensities for said blurred video image encompassing all pixels (j,k) in said

blurred video image and $u(n; c) = u(j,k;n;c)$ comprises a 2-D array of color c intensities for a restored image estimate at iteration number n.

12. (Previously Amended) The device of claim 7, wherein each group of said groups of said plurality of pixels comprises at least one pixel.

13. (Previously Amended) The device of claim 12, wherein said groups of said plurality of pixels comprises a group selected from 2 by 2 pixels, 3 by 3 pixels, and 4 by 4 pixels.

14. (Previously Amended) A device for deblurring a video image, comprising:

image means for providing a blurred video image comprising a plurality of pixels;

systolic array processor means for processing said blurred video image and adapted to download said blurred video image, said systolic array processor means comprising an array of processing logic block means in parallel for processing groups of said plurality of pixels in each processing logic block of said array of processing logic blocks respectively, wherein said processor means is adapted to sequentially exchange data between said array of processing logic block means by interconnecting said each processing logic block means with only a predefined number of processing logic block means adjacent thereto and wherein said systolic array processor means is adapted to provide an iterative update of said blurred video image by storing each pixel of said plurality of pixels in three planes within said systolic array processor means wherein said iterative update occurs within said blurred video image video frame update rate, and wherein said systolic array processor means includes means for uploading a deblurred video image.

15. (Previously Amended) The device of claim 14, wherein said three planes comprises said blurred video image, a blurred video image prediction error and a

past deblurred video image and wherein said systolic array processor means is adapted to provide an iterative update of said blurred video image by (i) providing feedback of said blurred video image prediction error using said deblurred video image and (ii) providing feedback of said past deblurred image video estimate.

16. (Previously Amended) The device of claim 15, wherein said systolic array processor means includes means for an iterative update implemented in said systolic array processing logic block means by $u(n + 1) = u(n) -- K *(H *u(n) -- y_b)--S* u(n)$ where u comprises an ideal undistorted image, m and n comprise column and row indices of an image pixel element, $y_b (m,n)$ comprises an observed blurred video image, * denotes convolution, K comprises a feedback update operator with a convolution kernel $k(m,n)$ and S comprises a smoothing operator with a convolution kernel $s(m.n)$.

17. (Previously Amended) The device of claim 16, wherein said operators H, K, and S are preloaded in said each processing logic blocks.

18. (Previously Amended) The device of claim 15, wherein said iterative update is implemented in said each processing logic block by $u(n + 1; c) = u(n; c) -- K *(H *u(n; c) -- y_b (c)) -- S * u(n;c)$ where $y_b (c) = y_d (j,k;c)$ comprises a 2-D array of color c intensities for said blurred video image encompassing all pixels (j,k) in said blurred video image and $u(n; c) = u(j,lc;n;c)$ comprises a 2-D may of color c intensities for a restored image estimate at iteration number n.

19. (Previously Amended) The device of claim 14, wherein each group of said groups of said plurality of pixels comprises at least one pixel.

20. (Previously Amended) The device of claim 19, wherein said groups of said plurality of pixels comprises a group selected from 2 by 2 pixels, 3 by 3 pixels and 4 by 4 pixels.

REMARKS

I. Claim Rejections - 35 USC § 103

Requirements for Prima Facie Obviousness

The obligation of the examiner to go forward and produce reasoning and evidence in support of obviousness is clearly defined at M.P.E.P. §2142:

> "The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

The U.S. Supreme Court ruling of April 30, 2007 (*KSR Int'l v. Teleflex Inc.*) states:

> "The TSM test captures a helpful insight: A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art. Although common sense directs caution as to a patent application claiming as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the art to combine the elements as the new invention does."
>
> "To facilitate review, this analysis should be made explicit."

The U.S. Supreme Court ruling states that it is important to identify a *reason* that would have prompted a person to combine the elements and to make that analysis *explicit*. MPEP §2143 sets out the further basic criteria to establish a *prima facie* case of obviousness:

1. a reasonable expectation of success; and

2. the teaching or suggestion of all the claim limitations by the prior art reference (or references when combined).

It follows that in the absence of such a *prima facie* showing of obviousness by the Examiner (assuming there are no objections or other grounds for rejection) and of a *prima facie* showing by the Examiner of a *reason* to combine the references, an applicant is entitled to grant of a patent. Thus, in order to support an obviousness rejection, the Examiner is obliged to produce evidence compelling a conclusion that the basic criterion has been met.

Biemond et al. in view of Owens et al., Lavenier and Okuda

The Examiner rejected claims 1-2, 5-8, 12-15, and 19-20 under 35 U.S.C. § 103(a) as being unpatentable over Biemond in view of Owens (citing "Computer Vision on the MGAP"), and in further view of Lavenier (citing "Advanced Systolic Design") and further in view of Okuda et al. (U.S. Patent No. 6,493,467) hereinafter referred to as "Okuda".

Regarding claim 1, the Examiner argued that Biemond describes an iterative method for image deblurring performed by a computing system used to process the image, but admitted Biemond does not explicitly teach the downloading of a video image, the use of a systolic array processor to perform the deblurring method. The Examiner argued that Owens teaches the downloading of an image for further processing (citing paragraph 2 of the "Introduction" section). The Examiner argued that Owens further teaches the use of a systolic array of interconnected logic blocks (Digital Processors) for the parallel processing of images (stating deblurring is image processing)(citing sections 2.1 and 3.1). The Examiner argued that Owens shows the adjacent interconnections of the processing array in which the plurality of pixels are communicated to their respective Digital Processors (processing logic blocks) (citing FIG. 4).

The Examiner argued that it would have been obvious to one of ordinary skill in the art at the time of the invention to use the known systolic array disclosed by Owens with the known iterative image deblurring method disclosed by Biemond

according to Lavenier that teaches the use of iterative methods on systolic array (citing Lavenier, section 5.2). The Examiner argued therefore that the combination provides the predictable result of iterative image deblurring according to the known method of Biemond using the known device of a systolic array as disclosed by Owens and Lavenier.

The Examiner admitted that neither Owens, nor Lavenier, nor Biemond discuss the processing of video images. However, the Examiner argued that a video is a series of frames (images) and a method such as is taught by Biemond that operates on a single image can clearly be used to operate on a plurality of images sequentially. Thus, the Examiner argued that the method taught by Biemond is view of Owens and Lavenier for deblurring an image can also be used on a sequence of images (video).

The Examiner argued that Biemond teaches the iterative deblurring method in the section entitled "Iterative Solutions" (citing Biemond, page 865) using three sets of data each dependent on the particular pixel data they correspond to (the Examiner argued that thus each set is an image "plane" because it varies with x and y, where x and y are the pixel indices). The Examiner argued that the method and system disclosed by Biemond in view of Owens and Lavenier correct the image at some rate but admitted they do not specify that it is at the frame rate of the video (i.e. real time). However, the Examiner argued that Okuda teaches a parallel processing system (citing Okuda col. 3, lines 29-24 and col. 97, lines 8-13) that performs real-time processing on image data by utilizing a parallel processing system.

The Examiner argued that thus, as evidenced by Okuda, one of ordinary skill in the art at the time of the invention would have expected the reduction in image processing time when utilizing a parallel processing system and would have desired the image processing to occur in real-time. The Examiner argued that therefore, it would have been obvious to one of ordinary skill in the art to modify the parallel processing system and method of Biemond, Owens and Lavenier with the teachings

of Okuda to process image data in real-time. The Examiner argued that real-time processing allows for real-time video processing since a video is a sequence of single images.

The Examiner admitted that Owens and Biemond do not explicitly teach the uploading of the blurred image. The Examiner takes official notice that the uploading of the deblurred (processed) image is notoriously well known in the art. The Examiner argued that since the purpose of deblurring the image is to produce a deblurred image for display or further processing, and thus would have been obvious to one of ordinary skill in the art to store or upload the processed image for retrieval or display.

The Applicant respectfully disagrees with this assessment and notes that the limitations of claim 1 as submitted before are not disclosed in the prior art. The Applicant's invention is a method and system for *deblurring* video images, wherein the video image is deblurred by the Applicant's invention one still image of the video image at a time wherein the image is deblurred such that the iterative update occurs within the video frame update rate. The cited prior art does not disclose this limitation.

The Examiner has admitted that the prior art does not disclose deblurring of a *video* image; one of the limitations of the Applicant's invention. The Examiner argues that video images are a series of frames and a method such as taught by Biemond which operates on a *single* image would operate on a *plurality* of images. The Examiner has not provided evidence of such a conclusion. The Examiner has included the Okuda reference in the current office action, stating that Okuda performs real-time processing on image data by utilizing a parallel processing system.

Okuda, however, does not disclose *deblurring* of a video image, as in the Applicant's invention. Okuda does indeed disclose processing of an image but defines this "processing" as color correction of the image, as shown in col. 1, lines 18-22 and col. 3, lines 22-28. The Examiner has not stated how the single image

deblurring methods of Biemond in view of Owens and Lavenier would combine with the color processing of Okuda to perform video image deblurring. The fact that Okuda may be able to process the color correction in a video at "real-time" does not make the combination of Okuda and Biemond in view of Owens and Lavenier a video image deblurring method. How would the Biemond in view of Owens and Lavenier method of deblurring *single* images be improved with the color correction method of Okuda? The Applicant respectfully submits that the Examiner's argument seems to be a statement that as color correction by Okuda is performed on video in real-time the method of Biemond in view of Owens and Lavenier may be also performed on video images without any supporting evidence that this would be possible.

The Applicant submits that the prior art references of Biemond and Owens only disclose methods on *single* images as high resolution images require significant computing power and require a significant amount of time to process. This makes it virtually impossible (utilizing the cited prior art methods) to deblur streaming video in *real time*; i.e. within the video frame update rate. The Examiner has argued that "a video is merely a sequence of still images", however, the Applicant respectfully submits that this statement is completely correct. If a video is nothing more than a sequence of still images, as submitted by the Examiner, then a "slide show" would qualify as a video also. The difference between a slide show, or a simple sequence of still images and a video is that the images must be displayed at a sufficiently fast rate such that a person would not perceive the individual images, perceiving only a "moving" image. Therefore, a "video image" is a sequence of still images displayed a t a sufficiently fast frame update rate that the still images are not perceived. Nothing disclosed in the Biemond, Owens or Lavenier references suggests that these methods, singularly or in combination, could be processed at a rate within the video frame update rate, or that these methods could even be utilized in deblurring video images. Okuda discloses color correction processing only and the Examiner has not stated how the combination would deblur video images within the video

frame update rate. The combination of the Biemond, Owens, Lavenier and Okuda references would not result in a video image deblurring method or system.

The Applicant submits that the Applicant's invention of claim 1 is not a predictable use or prior art elements according to their established functions. As the cited prior art discloses *deblurring* methods utilized on *single* images only, without any teaching or suggestion that the iterative update could be utilized to deblur *video* images or wherein the iterative update occurs *within* the blurred video image video frame update rate, the Applicant submits that the prior art combination does not provide a predictable result of the Applicant's invention.

The Examiner argued that the Applicant has made a broad statement that none of the rejections have a proper motivation for combination and that the Applicant has not specifically addressed what the issues with each of the proposed combinations and motivations are. The Applicant respectfully disagrees with this statement and quotes, for example, one argument for the combination from the Examiner's argument as follows:

> "It would have been obvious to one of ordinary skill in the art at the time of the invention to use the known systolic array disclosed by Owens with the known iterative image deblurring method disclosed by Biemond according to Lavenier that teaches the use of iterative methods on systolic array." (page 7 of the current office action).

The Applicant submits that the *specific issue* is that the Examiner has not provided any motivation or explicit reason for the combination. The Examiner has simply made a conclusory statement that it would be obvious to combine the references. For example, the Examiner has not provided an explicit reason (as required by the U.S. Supreme Court in *KSR v. Teleflex,* page 14) *why* one of ordinary skill in the art would have been prompted to combine the references as stated. The Applicant reminds the Examiner that it remains *legally insufficient* to conclude that a claim is obvious even if each element of the claim can be independently shown in the cited prior art (*KSR v. Teleflex*) as all innovation is a combination of known elements. This is exactly the Examiner's argument. The

Examiner has simply argued that some limitations are disclosed in Biemond, some further in Owens and Lavenier, and finally some more in Okuda. The Examiner thereafter concludes that therefore it would be obvious to combine the references. The Examiner has not provided any motivation or reason for the combination, merely stating the conclusory opinion that it would be obvious. The Examiner has argued that all of the limitations are disclosed in the 4 cited prior art references and therefore it is obvious. This is not a legal *prima facie* case of obviousness under the MPEP or the U.S. Supreme Court.

The U.S. Supreme Court has stated that some *articulated reasoning* with some *rationale underpinning* to support the legal conclusion of obviousness must be provided (*KSR v. Teleflex*, page 14), including identifying a reason that would have prompted a person of ordinary skill in the art to combine the elements as the claimed invention does. This rationale must be made *explicit* including a detailed explanation of the *background knowledge* possessed by a person having ordinary skill in the art at the time of the invention. Anything less than such an explicit analysis may not be sufficient to support a *prima facie* case of obviousness (*KSR v. Teleflex*, page 14).

The Examiner has not provided this explicit reasoning why one of ordinary skill in the art would combine the elements of the combination, as the Applicant's invention, for any of the 20 claims in the application, nor has the Examiner included a detailed explanation of the background knowledge possessed by a person having ordinary skill in the art. In all cases, the Examiner has simply argued that the limitations are disclosed in the cited prior art and "therefore" it is obvious to one of ordinary skill in the art.

Therefore, the Applicant submits that this same argument against a *prima facie* case of obviousness for lack of an explicit reasoning why one of ordinary skill in the art would combine the elements can be made for each claim in the application. Without this required reasoning, the Examiner has not made a *prima*

facie case of obviousness and the Applicant is entitled to a grant of a patent in accordance with MPEP §2143 and the U.S. Supreme Court, *KSR v. Teleflex*.

The Examiner has not stated that the prior art discloses the limitation of each processing block exchanges data *only* with *adjacent* processing blocks, merely stating that the limitation is the definition of array processing. The Applicant respectfully disagrees with this assessment noting that the Applicant's limitation is that the processing array exchanges data *only* with the adjacent processing block. This is not the definition of array processing and this limitation of only exchanging data with adjacent processing blocks is not disclosed in the cited prior art references. The Examiner argued that Owens discloses a systolic array *connected* to only a predetermined number of adjacent blocks (item 4, response to arguments); however, the limitation of the Applicant's claim is that the processing blocks *exchange* data only with adjacent blocks. This is not the same and has not been submitted as disclosed in the prior art. Therefore the Applicant's limitation is not disclosed in Owens.

Therefore, Biemond in view of Owens, Lavenier and Okuda does not disclose the limitations of: 1) deblurring a *video* image, 2) providing an iterative update of the blurred *video* image within the blurred video image video frame update rate, and 3) wherein each processing block exchanges data *only* with adjacent processing blocks.

Therefore, Biemond in view of Owens, Lavenier and Okuda fails in the aforementioned *prima facie* obviousness test as each and every limitation of the Applicant's claim 1 is not disclosed. Additionally, the Examiner has not provided any explicit reason to combine the Biemond, Owens, Lavenier and Okuda references.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claim 1 based on the Biemond, Owens, Lavenier and Okuda references be withdrawn.

Regarding claim 2, the Examiner argued that Owens and Lavenier disclose the implementation of an iterative method on a systolic array as is discussed in

rejection of claim 1. The Examiner argued that Biemond teaches an iterative method for deblurring images (citing Biemond, pages 865-868 under the section titled "C. Iterative Solutions") using error feedback and past deblurred image estimate feedback (citing equations 56 and 57 on page 865). Furthermore, the Examiner argued that as evidenced by Lavenier (citing Lavenier section 5.2), the implementation of iterative algorithms on a processing array was well known to one of ordinary skill in the art.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejection of claim 1 applies equally against the rejection of dependent claim 2.

Therefore, Biemond in view of Owens, Lavenier and Okuda fails in the aforementioned *prima facie* obviousness test as each and every limitation of the Applicant's claim 2 is not disclosed. Additionally, the Examiner has not provided any motivation to combine Biemond in view of Owens, Lavenier and Okuda references nor has the Examiner made an explicit reasoning why one of ordinary skill in the art would combine the references.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejection of claim 2 based on Biemond in view of Owens, Lavenier and Okuda be withdrawn.

Regarding claim 5, the Examiner argued that Biemond in view of Owens and Lavenier, as applied to claim 1, teach the deblurring of an image using a systolic processor array. The Examiner argued that Owens teaches the implementation of image processing methods using systolic array processors for image processing (citing Owens, final line of the second paragraph on page 338) that at a least one pixel is operated on per processor. Thus, the Examiner argued that, as is taught by Owens, the pixels are grouped into groups of pixels such that at least one pixel is operated on per processor.

Regarding claim 6, the Examiner argued that filtering and image processing methods such as deblurring are done locally by operating on groups of adjacent

pixels. The Examiner argued that Owens discloses an example of such a grouping (citing Owens section 3.1 on page 338) wherein Owens disclosed the use of 3x3 masks applied to the image and hence it was known to group and process pixels in a processing array.

The Examiner argued that claims 7-8, 12-13, 14-15, and 19-20 claim the corresponding device that performs the method of claims 1-2, and 5-6. The Examiner argued that as per the rejections of claims 1-2 and 5-6, the method has been disclosed by Biemond in view of Owens and Lavenier. Furthermore, the Examiner argued that the device has been disclosed since Owens and Lavenier have disclosed the implementation of such methods on a systolic array device.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejection of claim 1 applies equally against the rejection of claims 5-8, 12-15 and 19-20.

Therefore, Biemond in view of Owens, Lavenier and Okuda fails in the aforementioned *prima facie* obviousness test as each and every limitation of the Applicant's claims 5-8, 12-15 and 19-20 is not disclosed. Additionally, the Examiner has not provided any motivation to combine Biemond in view of Owens, Lavenier and Okuda nor has the Examiner made an explicit reasoning why one of ordinary skill in the art would combine the references.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 5-8, 12-15 and 19-20 based on Biemond in view of Owens, Lavenier and Okuda be withdrawn.

Biemond in view of Owens, Lavenier, Okuda and Gorinevsky

The Examiner rejected claims 3, 9-10, and 16-17 under 35 U.S.C. § 103(a) as being unpatentable over Biemond in view of Owens, Lavenier and Okuda as applied to claims 1-2 and 5 above, and in further view of Gorinevsky (citing "Optimization-based Tuning of Low-bandwidth Control in Spatially Distributed Systems").

Regarding claim 3, the Examiner argued that Biemond identifies the existence of regularization error and discloses a solution of the regularization error (citing Biemond section 5, page 868). The Examiner argued that the term S*u(n) as defined by applicant was known to one of ordinary skill in the art as a solution to the regularization problem. The Examiner admitted that Biemond does not teach the regularization method shown by applicant. However, the Examiner argued that Gorinevsky (citing Gorinevsky sections 1 and 3) teaches a filter that improves the spatial response (reduces regularization error) of the system. The Examiner argued that it would have been obvious to one of ordinary skill in the art to substitute the regularization method as taught by Gorinevsky for the regularization method taught by Biemond with a reasonable expectation of success while maintaining or improving the spatial response (reduction of regularization error) provided by the method taught by Biemond. Furthermore, the Examiner argued that in the same sections of Gorinevsky, the use of the term K has also been disclosed.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejection of claim 1 applies equally against the rejection of dependent claim 3. Additionally, Biemond in view of Owens, Lavenier, Okuda and Gorinevsky does not disclose the limitations of claim 3.

The Examiner has admitted that Biemond does not utilize or disclose the algorithm in the method of claim 3, however, the Examiner argues that the term S*u(n) is known as a solution to the regularization problem and Gorinevsky teaches a filter that improves the spatial response of the system. The Examiner continues, stating that Gorinevsky teaches the term K. The Examiner does not state that this is the same algorithm as in claim 3, however. Specifically, the algorithm: $u(n + 1) = u(n) - K *(H *u(n) - y_b) - S * u(n)$ is not disclosed in the prior art and the Examiner has not stated or argued that it *is* disclosed. Individual components of the may be disclosed in the references, but the algorithm itself is not disclosed. The Examiner has simply stated that as the components are disclosed it would be obvious to combine to somehow result in the Applicant's algorithm. Without the

algorithm disclosed in the prior art, either singularly or in combination, a *prima facie* case of obviousness has not been made.

Therefore, Biemond in view of Owens, Lavenier, Okuda and Gorinevsky fails in the aforementioned *prima facie* obviousness test as each and every limitation of the Applicant's claim 3 is not disclosed. Additionally, the Examiner has not provided any motivation to combine the Biemond, Owens, Lavenier, Okuda and Gorinevsky references nor has the Examiner made an *explicit* reasoning why one of ordinary skill in the art would combine the references.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claim 3 based on the Biemond, Owens, Lavenier, Okuda and Gorinevsky references be withdrawn.

The Examiner argued that claims 9 and 16 claim the corresponding device that performs the method of claim 3. The Examiner argued that as per the rejections of claims 1-3, the method has been disclosed by Biemond in view of Owens, Lavenier, Okuda and Gorinevsky.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejection of claim 1 applies equally against the rejection of claims 9 and 16.

Therefore, Biemond in view of Owens, Lavenier, Okuda and Gorinevsky fails in the aforementioned *prima facie* obviousness test as each and every limitation of the Applicant's claims 9 and 16 is not disclosed. Additionally, the Examiner has not provided any motivation to combine the Biemond, Owens, Lavenier, Okuda and Gorinevsky references nor has the Examiner made an explicit reasoning why one of ordinary skill in the art would combine the references.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 9 and 16 based on the Biemond, Owens, Lavenier, Okuda and Gorinevsky references be withdrawn.

Regarding claims 10 and 17, the Examiner admitted that Owens and Lavenier do not explicitly teach the preloading of the information into each

processing logic block of the array. However, the Examiner argued that as is evidenced by Owens (citing Owens second paragraph of page 338) the addition, subtraction, multiplication,...,etc. are performed on the received pixel data. The Examiner argued that in order to perform these operations the values intended to be used in these operations must be stored in the processing elements. Furthermore, the Examiner argued that as per the disclosure of Lavenier (citing Lavenier section 5.2) the weights of matrix W are stored in the processing units so that they can be used to multiply the values of the input (X). Thus, the Examiner argued that it is clear from this disclosure that known constants are stored in the processing units (logic blocks) in order to perform the predetermined operations.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejection of claim 1 applies equally against the rejection of claims 10 and 17.

The Examiner has admitted that the prior art references do not disclose the claim 10 and 17 limitations merely stating that other values are stored in the processing blocks. The Examiner does not try to explain how it would be obvious to one of ordinary skill in the art to preload the operators H, K and S into each processing logic block of the array.

Therefore, Biemond in view of Owens, Lavenier, Okuda and Gorinevsky fails in the aforementioned *prima facie* obviousness test as each and every limitation of the Applicant's claims 10 and 17 is not disclosed.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 10 and 17 based on the Biemond, Owens, Lavenier, Okuda and Gorinevsky references be withdrawn.

Biemond in view of Owens, Lavenier, Gorinevsky and Dowski

The Examiner rejected claims 4, 11, and 18 under 35 U.S.C. §103(a) as being unpatentable over Biemond in view of Owens, Lavenier, Okuda and

Gorinevsky as applied to claims 3, 9-10, and 16-17 in further view of Dowski (U.S. Patent Publication No. 2003/0169944).

Regarding claim 4, the Examiner argued that claim 4 is a modification of the method of claim 3 wherein the deblurring is performed on each color space separately. The Examiner argued that Biemond discusses image processing, but admitted Biemond does not go into the particulars of color space processing. However, the Examiner argued that as evidenced by Dowski (citing Dowski paragraph [0018]) the method of dividing an image into its color spaces and then deblurring each of the color spaces was known to one of ordinary skill in the art. Furthermore, the Examiner argued that the teaching of Dowski shows that one of ordinary skill in the art knew how to apply image-filtering processes such as deblurring to each color channel. The Examiner argued that given that Biemond teaches the deblurring of at least a grayscale image and that Dowski teaches the application of a single channel deblurring process to each of the color channels. The Examiner argued that it would have been obvious to one of ordinary sill in the art to combine the teachings of Dowski with Biemond to perform the deblurring technique as taught by Biemond on each channel of a color image (citing as taught by Dowski) and yield the expected result of a deblurred color image.

The Examiner argued that claims 11 and 18 claim the corresponding device that performs the method of claim 4. The Examiner argued that as per the rejections of claims 1-4, the method has been disclosed by Biemond in view of Owens, Lavenier, Gorinevsky, Okuda and Dowski. Furthermore, the Examiner argued that the device has been disclosed since Owens and Lavenier have disclosed the implementation of such methods on a systolic array device.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejection of claim 1 applies equally against the rejection of dependent claims 4, 11 and 18.

Therefore, Biemond in view of Owens, Lavenier, Okuda, Gorinevsky and Dowski fails in the aforementioned *prima facie* obviousness test as each and every limitation of the Applicant's claims 4, 11 and 18 is not disclosed.

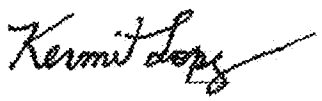
Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 4, 11 and 18 based on the Biemond, Owens, Lavenier, Gorinevsky, Okuda and Dowski references be withdrawn.

III. Conclusion

In view of the foregoing discussion, the Applicant has responded to each and every rejection of the Official Action. The Applicant has clarified the structural distinctions of the present invention. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §103 based on the preceding remarks. Reconsideration and allowance of Applicant's application is also respectfully solicited.

Should there be any outstanding matters that need to be resolved, the Examiner is respectfully requested to contact the undersigned representative to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,



Dated: October 2, 2008

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